What is claimed is:

1. A method of providing electrostatic discharge protection for an integrated circuit, comprising:

mounting an integrated circuit die on a lead frame;

encapsulating at least part of the integrated circuit die with a plastic or epoxy material; and

folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material.

2. The method of claim 1, further comprising:

connecting the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material to a ground voltage.

3. The method of claim 1, wherein the step of encapsulating at least part of the integrated circuit die with a plastic or epoxy material further comprising:

after mounting the integrated circuit die on the lead frame, encapsulating exposed surfaces of the integrated circuit die except for a sensing surface; and

encapsulating wire bonds connecting the integrated circuit die to portions of the lead frame.

4. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around each side of the encapsulated integrated circuit die.

5. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a first side of the encapsulated integrated circuit die, wherein the first portion includes an opening providing access for a connector to pins electrically connected to the integrated circuit die.

6. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding portions of the lead frame around edges of the encapsulated integrated circuit die not including leads electrically connected to the integrated circuit die.

7. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die.

8. The method of claim 1, wherein the step of folding a portion of the lead frame around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral

upper surface of the plastic or epoxy material further comprising:

folding a first portion of the lead frame around a side of the encapsulated integrated circuit die; and

folding a second portion of the lead frame extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

9. An integrated circuit package, comprising:

an integrated circuit die mounted on a lead frame; and

a plastic or epoxy material encapsulating at least part of the integrated circuit die,

wherein a portion of the lead frame is folded around sides of the encapsulated integrated circuit die and over or adjacent to a peripheral upper surface of the plastic or epoxy material.

10. The integrated circuit package of claim 9, further comprising:

a connection between a ground voltage and the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material.

11. The integrated circuit package of claim 9, wherein the plastic or epoxy material encapsulates exposed surfaces of the integrated circuit die except for a sensing surface and wire bonds connecting the integrated circuit die to portions of the lead frame.

12. The integrated circuit package of claim 9, wherein portions of the lead frame are folded around each side of the encapsulated integrated circuit die.

13. The integrated circuit package of claim 9, wherein a first portion of the lead frame folded around a first side of the encapsulated integrated circuit die includes an opening providing access for a connector to pins electrically connected to the integrated circuit die.

14. The integrated circuit package of claim 9, wherein portions of the lead frame are folded only around edges of the

encapsulated integrated circuit die not including leads electrically connected to the integrated circuit die.

15. The integrated circuit package of claim 9, wherein:

a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and

a second portion of the lead frame extending from the first portion is folded over a peripheral upper surface of the encapsulated integrated circuit die.

16. The integrated circuit package of claim 9, wherein:

a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and

a second portion of the lead frame extending from the first portion is folded adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die.

17. An integrated circuit package, comprising:

a lead frame including a die paddle and portions extending from the die paddle;

an integrated circuit die mounted on the die paddle;

a plastic or epoxy material encapsulating exposed surfaces of the integrated circuit die except for a sensing surface,

wherein the portions of the lead frame extending from the die paddle are folded around sides of the encapsulated integrated circuit die and over or adjacent to peripheral upper surfaces of the encapsulated integrated circuit die.

18. The integrated circuit package of claim 17, wherein the lead frame includes pins or leads and the portions extending from the die paddle include openings around the pins or leads.

19. The integrated circuit package of claim 17, wherein the lead frame includes pins or leads and the portions extending from the die paddle project from peripheral edges of the die paddle not adjacent to the pins or leads.

20. A lead frame strip for an integrated circuit package, comprising:

at least one lead frame, the lead frame including:

a die paddle on which an integrated circuit will be mounted;

a plurality of structures which will be formed into pins or leads for the integrated circuit package; and

portions extending from the die paddle which will be folded around sides of the integrated circuit package and over or adjacent to a peripheral upper surface of the integrated circuit package to form an electrostatic discharge ring.